IN THE CLAIMS:

Claims 1, 11, 16 and 32-35 have been amended herein. All of the pending claims 1 through 40 are presented, pursuant to 37 C.F.R. §§ 1.121(c)(1)(i) and 1.121(c)(3), in clean form below. Please enter these claims as amended. Attached is a marked-up version of the claims amended herein pursuant to 37 C.F.R. § 1.121(c)(1)(ii).

1. (Amended) A method for interconnecting at least two semiconductor dice, comprising:

providing a first semiconductor die including a plurality of bond pads arranged in an array over an active surface thereof;

providing at least one second semiconductor die including a plurality of bond pads on an active surface thereof;

orienting said first semiconductor die and said at least one second semiconductor die with said active surfaces thereof facing each other;

electrically connecting at least some bond pads of said plurality of bond pads of said at least one second semiconductor die with corresponding bond pads of said plurality of bond pads of said first semiconductor die.

2. The method of claim 1, wherein said providing said first semiconductor die comprises providing a logic die.

3. The method of claim 1, wherein said providing said at least one second semiconductor die comprises providing at least one memory device.

4. The method of claim 1, wherein said electrically connecting comprises providing conductive structures directly between said plurality of bond pads of said at least one second semiconductor die and said corresponding bond pads of said first semiconductor die.

5. The method of claim 4, wherein said providing conductive structures comprises providing balls, bumps, columns, or pillars comprising conductive material.

6. The method of claim 4, wherein said providing conductive structures comprises providing structures formed from a material comprising at least one of a metal, an alloy, a conductive epoxy, a conductor-filled epoxy, and a z-axis conductive elastomer.

7. The method of claim 1, further comprising aligning said at least some bond pads of said at least one second semiconductor die with said corresponding bond pads of said first semiconductor die.

8. The method of claim 1, wherein, upon said orienting, other bond pads of said plurality of bond pads of said first semiconductor die remain exposed beyond an outer periphery of said at least one second semiconductor die.

9. The method of claim 8, further comprising:
providing a carrier including a plurality of contacts;
orienting said first semiconductor die with said active surface thereof facing said carrier; and
electrically connecting said other bond pads of said first semiconductor die to corresponding contacts of said carrier.

10. The method of claim 9, wherein said providing said carrier comprises providing a carrier substrate with said plurality of contacts comprising contact pads located on a surface thereof.

a4 11. (Amended) The method of claim 10, wherein said providing said carrier substrate comprises providing said carrier substrate with at least one recess formed in said surface.

12. The method of claim 11, wherein said orienting includes at least partially disposing said at least one second semiconductor die in said at least one recess.

13. The method of claim 9, wherein said providing said carrier comprises providing leads corresponding to each of said other bond pads.

14. The method of claim 9, wherein said electrically connecting said other bond pads of said first semiconductor die to said corresponding contacts of said carrier comprises disposing conductive elements between said other bond pads and said corresponding contacts.

15. The method of claim 14, wherein said disposing conductive elements comprises providing at least one of balls, bumps, columns, and pillars comprising conductive material between each of said other bond pads and said corresponding contacts.

16. (Amended) The method of claim 14, wherein said disposing said conductive elements between said other bond pads of said first semiconductor die and said corresponding contacts of said carrier comprises providing a quantity of a material comprising at least one of a metal, an alloy, a conductive epoxy, a conductor-filled epoxy, and a z-axis conductive elastomer.

17. The method of claim 10, wherein said providing said first semiconductor die comprises providing said first semiconductor die with a first member of a conductive element secured to each other bond pad thereof and wherein said providing said carrier substrate comprises providing said carrier substrate with a second member of said conductive element secured to each corresponding contact pad thereof.

18. The method of claim 17, further comprising aligning at least said first and second members of said conductive element.

19. The method of claim 18, further comprising securing at least said first and second members of said conductive element to each other.

20. The method of claim 17, further comprising providing a conductive mating structure bearing a third member of said conductive element between said first semiconductor die and said carrier substrate.

21. The method of claim 20, further comprising aligning said first, second, and third members of said conductive element.

22. The method of claim 21, further comprising securing said first, second, and third members of said conductive element to one another.

23. A method for packaging a semiconductor device assembly, comprising:

providing a first semiconductor die including a plurality of bond pads arranged in an array over an active surface thereof;

providing at least one second semiconductor die including a plurality of bond pads arranged on an active surface thereof;

orienting said at least one second semiconductor die over said first semiconductor die with said active surface facing said active surface of said first semiconductor die, said plurality of bond pads of said at least one second semiconductor die in alignment with corresponding bond pads of said first semiconductor die;

providing a carrier with a plurality of contacts; and

orienting said first semiconductor die over said carrier with said active surface facing said carrier, bond pads of said first semiconductor die exposed beyond an outer periphery of said at least one second semiconductor die in alignment with corresponding contacts of said carrier.

24. The method of claim 23, further comprising electrically connecting said plurality of bond pads of said at least one second semiconductor die to said corresponding plurality of bond pads of said first semiconductor die.

25. The method of claim 23, further comprising electrically connecting bond pads of said first semiconductor die exposed beyond said outer periphery of said at least one second semiconductor die to said corresponding contacts of said carrier.

26. The method of claim 23, further comprising disposing a quantity of encapsulant material over at least said active surface of said first semiconductor die.

27. The method of claim 26, wherein said disposing said quantity of encapsulant material comprises disposing underfill material between said first semiconductor die and said carrier.

28. The method of claim 26, wherein said disposing said quantity of encapsulant material comprises substantially covering at least said first semiconductor die.

29. The method of claim 23, wherein said providing said carrier comprises providing a carrier substrate with said plurality of contacts comprising contact pads located on a surface thereof.

30. The method of claim 29, wherein said providing said carrier substrate comprises providing a carrier substrate with at least one recess formed in said surface.

31. The method of claim 30, wherein said orienting said first semiconductor die comprises at least partially disposing said at least one second semiconductor die within said at least one recess.

32. (Amended) The method of claim 23, wherein said providing said carrier comprises providing a plurality of leads, each of said plurality of leads corresponding to said bond pads of said first semiconductor die exposed beyond said outer periphery of said at least one second semiconductor die.

33. (Amended) The method of claim 29, wherein:

said providing said first semiconductor die comprises providing said first semiconductor die with a first member of a conductive element secured to each bond pad thereof that is located beyond said outer periphery of said at least one second semiconductor die; and

said providing said carrier substrate comprises providing said carrier substrate with a second member of said conductive element secured to each corresponding contact pad thereof.

34. (Amended) The method of claim 33, further comprising aligning at least said first and second members of said conductive element.

35. (Amended) The method of claim 34, further comprising securing at least said first and second members of said conductive element to each other.

36. The method of claim 33, further comprising providing a conductive mating structure bearing a third member of said conductive element between said first semiconductor die and said carrier substrate.

37. The method of claim 36, further comprising aligning said first, second, and third members of said conductive element.

38. The method of claim 37, further comprising securing said first, second, and third members of said conductive element to one another.

39. A method for packaging a semiconductor device assembly, comprising:

providing at least a first multi-chip module including:

a first semiconductor die with a plurality of bond pads arranged in an array over an active surface thereof; and

at least one second semiconductor die including a plurality of bond pads arranged on an active surface thereof, each of said plurality of bond pads of said at least one second semiconductor die in alignment with corresponding bond pads of said first semiconductor die, said active surfaces of said first semiconductor die and said at least one second semiconductor die facing one another, and said bond pads of said at least one second semiconductor die electrically connected to said corresponding bond pads of said first semiconductor die, other bond pads of said first semiconductor die exposed laterally beyond an outer periphery of said at least one second semiconductor die;

providing a carrier including contacts; and

orienting said at least said first multi-chip module over said carrier with said active surface of said first semiconductor die facing said carrier and said other bond pads in alignment with corresponding contacts of said carrier.

40. The method of claim 39 further comprising:

providing at least a second multi-chip module including:

a first semiconductor die with a plurality of bond pads arranged in an array over an active surface thereof; and

at least one second semiconductor die including a plurality of bond pads arranged on an active surface thereof, each of said plurality of bond pads of said at least one second semiconductor die in alignment with corresponding bond pads of said first semiconductor die, said active surfaces of said first semiconductor die and said at least one second semiconductor die facing one another, and said bond pads of said at least one second semiconductor die electrically connected to said corresponding

bond pads of said first semiconductor die, other bond pads of said first semiconductor die exposed laterally beyond an outer periphery of said at least one second semiconductor die; and

orienting said at least said second multi-chip module over said carrier with said active surface of said first semiconductor die facing said carrier and said other bond pads in alignment with corresponding contacts of said carrier.